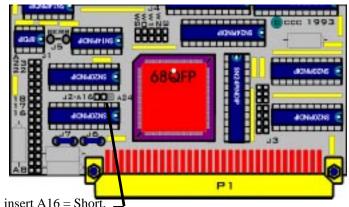
	VBD SERIES ADDRESS MAP													
HEX	A	ddre	ss B	its	Input Cha (S-D, R-D		Output Channels (D-S, D-R etc.)							
Select	<b>A</b> 4	<b>A</b> 3	A2 .	<b>A</b> 1	Function	Chan#	Function	Chan#						
00h	0	0	0	0		0		0						
02h	0	0	0	1		1	Write Chan.	1						
04h	0	0	1	0		2	, , , , , , , , , , , , , , , , , , ,	2						
06h	0	0	1	1		3		3						
08h	0	1	0	0	Read/Write Chan.	4		0						
0Ah	0	1	0	1		5	Readback	1						
0Ch	0	1	1	0		6	Channel	2						
0Eh	0	1	1	1		7		3						
*10h	1	0	0	0	D 10.	0 & 4	*-WS Units, A	ny Word						
12h	1	0	0	1	Read Status Chan.	1 & 5	here to Write 30	_						
14h	1	0	1	0		2 & 6	Self-Test Ang whole ca	-						
16h	1	0	1	1		3 & 7	whole ca	ıu						



J2: insert A16 = Short, insert A24 = Std.

Base Address Select, J1 Jumpers = A0 - A23 Address Bits, in = 0, out = 1																	
A					4	5		A 5					5		0	0	
1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	0000	0
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	A7-A0	Base

P2	PIN TERMINATIONS: VBR, VBW, VBD Series Units Front Panel Connectors P3 & P4  Disregard unused channels if not in your part number. (c) CCC 1997, 1999											
P2 Pins	P3 Pins	VBD	SERIES High Density	VBW/VBR Units * = QM Option			P4 Pins	VBD	SERIES High Density	VBR/VBW * = QM O		P2 Pins
C6	9	RH	Reference	-8 units RH/RL 0	RH		9	RH	Reference	-8 units	RH	C18
A6	28	RL	Kelefelice		RL		28	RL	Reference	RH/RL 2	RL	A18
A5	10	<b>S</b> 1		If used as	S1	ved	10	S1		If used as	S1	A17
A2	13	S2	Signals Channel	Multispeed:,	S2	esei	13 S2 Signals Channel	Multispeed:,	S2	A14		
C5	29	S3	0	chan.'s 0, 4 are Fine,	S3	Copyright CCC 1999, All Rights Reserved	29	S3	2	chan.'s 2, 6 are Fine,	S3	C17
C2	32	S4		Pair with	S4	ght	32	S4	1	Pair with	S4	C14
C4	30	<b>S</b> 1		chan.'s 2,5	*B-	l Ri	30	S1		chan.'s 3,7	*B-	C16
C3	31	S2	Signals Channel	= coarse & Read or Write In Succession	*B+	Al	31	S2	Signals Channel		*B+	C15
A4	11	<b>S</b> 3	4		*A-	999,	11	S3	6		*A-	A16
A3	12	S4			*A+	CIG	12	S4			*A+	A15
A1	15	OPT.	Vel.0 or RL4	-8 units	*M+		15	OPT.	Vel.2 or RL6	-8 units	*M+	A13
C1	34	OF I.	Vel.4 or RH4	RH/RL 4	*M-	M- 34 OP 1. Vel.6 or RH		Vel.6 or RH6	RH/RL 6	*M-	C13	
C12	1	RH	Deference	-8 units	RH	yrig	1	RH	Deference	-8 units RH/RL 3	RH	C24
A12	20	RL	Reference	RH/RL 1	RL	Zop.	20	RL	Reference		RL	A24
A11	2	S1		If used as	S1		2	S1	Signals Channel	If used as Multispeed:, chan.'s 2, 6 are Fine, Pair with	S1	A23
A8	5	S2	Signals Channel	Multispeed:, chan.'s 0, 4 are Fine, Pair with	S2	<i>"</i>	5	S2			S2	A20
C11	21	S3	1		S3	atio	21	S3			S3	C23
C8	24	S4			S4	oor	24	S4			S4	C20
C10	22	S1		chan.'s 2,5 = coarse & Read or Write In	*B-	Corp	22	S1	Signals Channel	chan.'s 3,7 = coarse & Read or Write In	*B-	C22
C9	23	S2	Signals Channel		*B+	—   ≋	23	S2			*B+	C21
A10	3	S3	5		*A-		3	S3			*A-	A22
A9	4	S4		Succession	*A+	ıveı	4	S4	1	Succession	*A+	A21
A7	7	ODT	Vel.1 or RL5	-8 units	*M+	Cor	7	ODT	Vel.3 or RL7	-8 units	*M+	A19
C7	26	OPT.	Vel.5 or RH5	RH/RL 5	*M-	ter	26	OPT.	Vel.7 or RH7	RH/RL 7	*M-	C19
	18	+12V	If ext. supplies	-12 units are		ndu	18	+12V	If ext. supplies	-12 units ar		
1 1	36,37	GND	Power Ground	12VDC Bus or Ext., Otherwise +/-15		Co	36,37	GND	Power Ground	- 12VDC Bus or Ext., Otherwise +/-15		
1 1	19	-12V	If ext. supplies	VDC Ex			19	-12V	If ext. supplies	VDC Ex		
P2	6,25,14, & 33 DC COMMON		DC (	Common		I	4, & 33 DC IMON	DC (	Common		P2	
	P3 & P4 Connector AMP #745784-4, Mates: TRW/CINCH # DC-37P Included P3 & P4 Connector AMP #745784-4, Mates: TRW/CINCH # DC-37P Included											

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### **ADDRESSING**

The physical module address is decoded by setting Address Select Jumpers for the desired AM code (address modifier) and base address (board select). Jumper plug installed equals logic "0".

# **ADDRESSING RANGE**

CCC VME Modules are configured for the A24 standard addressing over a 16M byte range, two shunt jumpers are provided to permit A16 short addressing over a 64K byte range.

### **A24 MODE:**

Uses address lines A01-A023. Jumper (J2) is inserted in the A24 position and jumper A16 (J3) is removed to allow standard addressing over a full 16M byte range.

Client may use the following Am codes (address modifiers):

"3D" Standard supervisory Data Access or,

"39" Standard Non-Privileged Data Access

#### A16 MODE:

Uses address lines A01-A015. Jumper (J2) is inserted in the A16 position and jumper A16 (J3) is installed to allow short addressing over a 64K byte range. Client may use the following AM codes:

"2D" short supervisory I/O Access or,

"29" short Non-Privileged I/O Access.

The base address may be set up via reliable shunt plugs anywhere on the 256 byte boundaries.

### **NOTES:**

- 1) **READ BACK:** If channel zero is a primarily write converter function (ie: Digital to Synchro); then "00" in Hex is the address to Write the New Command Word, and "08" in Hex is the address to "READ-BACK' the Command Word for verification.
- 2) **READ STATUS:** This is a separate status register used for each module for fault and VME I/O Card configuration information.
- On **High Density "VBD"** modules one status register is used for every two converters; they are paired per status register as channels 0 & 4, 1 & 5, 2 & 6, 3 & 7. all status bits apply equally to each channel with individual Fault/Bite Status bits for each respective channel.
- 3) **DTACK:** The CCC DTACK response is less then 9 VME Bus clock cycles for standard units, less then 14 for channels 4-7.
- 4) All CCC VME Bus cards are register based A24:D16 slave devices. All converters used are independent (not multiplexed) continuously tracking signal input converters, and independent continuously updated signal output converters.

These independent channels can be addressed and either written to, or read from, without any special timing considerations, specialized timing algorithms, or interrupts. The user simply addresses the channel, and reads or writes the data.

# **VME BUS I/O Cards**

# Addressing, Status Word and Control word Details

### STATUS WORD & CONTROL WORD DETAILS

St	Status Word, Lower Byte (Higher Byte Not Used)											
	ST	PF	F1	F2	F3	MP	W	R				
Bits	D7	D6	D5	D4	D3	D2	D1	D0				

**Status Word (Read Functions):** 

1 status word per channel upto 4 channel units, 1 status word per every 2 channels on VBD units.

Bit D0: 0 = Read Channel:

This channel is configured for a Read Command. ex: Synchro to Digital or A to D.

**Bit D1: 0 = Write Channel:** 

This channel is configured for a write command.

ex: Digital to Synchro or D to A

\*If both bits D0 and D1 are logic 1, this indicates no active module. \*If both bits D0 and D1 are logic 0, = configuration - Jumper error.

### Bit D2: 0 = Multi-Pair:

This channel is paired with adjacent channel for a multispeed or Multiturn operation.

Channels 0 and 1, (4 and 5 Hi-Den)= Multi-pair #0,1

Channels 2 and 3, (6 and 7 Hi-Den)= Multi-pair #2,3

The paired channels should be read in succession.

Not used on boards with multispeed converters.

**Bit D3 : 1** = Converter Busy, (F3 Fault) not required to be polled, all cards insure valid data is always read by the bus.

Bit D4: <sup>1</sup>Converter Fault Channels 0,1,2, and 3

Bit D5: <sup>1</sup>Converter Fault Channels 4,5,6, and 7 (VBD units)

<sup>1</sup>Loss of Reference, Loss of Signal, overspeed/accel. & conv. fault. If converter is given a large simulated step input stays untill settled.

Bit D6: 0 = Power Fail, loss of +/-15 or +/-12VDC supplies.

Bit D7: 1 = In Self Test Mode, all input converters should be reading 30° test angle +/-.15°. (-WS models only, else ignore).

## **Control Word (Write Self Test): (-WS Models Only)**

Control words compliment the status word address locations. Activating or de-activating the self-test mode by setting Bit D7 high = 1in any of these locations will put the card into (or out of) the self test mode.

Bit D7: 1 = Force into Self Test Mode, all input converters will internally disconnect their input signals and instead switch to read an anolog simulated  $30^{\circ}$  test angle for a confirmation test.

When activated look at the converter fault bits indicating when ready to read, if not settled (unfaulted) within 2 seconds = failed.

Proceed by comparing the data read on each channel to  $30^{\circ}$  +/- .15°. When done set to 0 to activate the run mode, again check fault bits in the status word to make sure the converters are settled.

Bit D7: 1 = Force into Run Mode, normal operation.